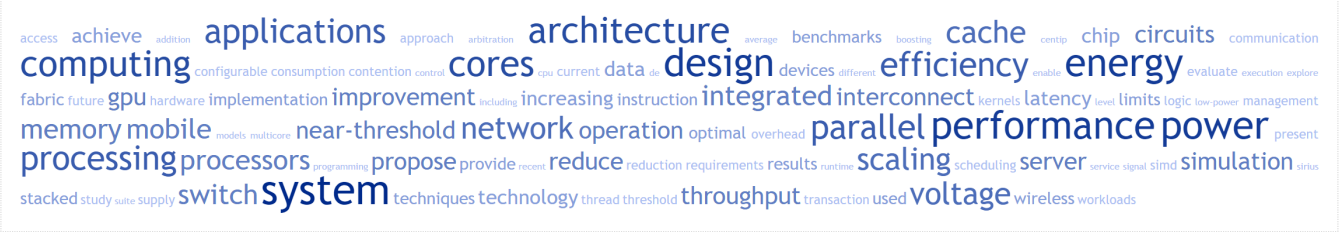
Publications



Heterogeneity-Aware Scheduling on SoCs for Autonomous Vehicles.
Aporva Amarnath, Subhankar Pal, Hiwot Tadese Kassa, Augusto Vega, Alper Buyuktosunoglu, Hubertus Franke, John-David Wellman, Ronald Dreslinski Jr., Pradip Bose:

Heterogeneity-Aware Scheduling on SoCs for Autonomous Vehicles. IEEE Comput. Archit. Lett. 20(2): 82-85 (2021)

A Survey Describing Beyond Si Transistors and Exploring Their Implications for Future Processors.
Heewoo Kim, Aporva Amarnath, Javad Bagherzadeh, Nishil Talati, Ronald G. Dreslinski:
A Survey Describing Beyond Si Transistors and Exploring Their Implications for Future Processors. ACM J. Emerg. Technol. Comput. Syst. 17(3): 27:1-27:44 (2021)

An Ultra-Low-Power Image Signal Processor for Hierarchical Image Recognition With Deep Neural Networks.
Hyochan An, Sam Schiferl, Siddharth Venkatesan, Tim Wesley, Qirui Zhang, Jingcheng Wang, Kyojin Choo, Shiyu Liu, Bowen Liu, Ziyun Li, Luyao Gong, Hengfei Zhong, David T. Blaauw, Ronald G. Dreslinski, Hun-Seok Kim, Dennis Sylvester:
An Ultra-Low-Power Image Signal Processor for Hierarchical Image Recognition With Deep Neural Networks. IEEE J. Solid State Circuits 56(4): 1071-1081 (2021)

Applications of Artificial Intelligence on the Modeling and Optimization for Analog and Mixed-Signal Circuits: A Review.
Morteza Fayazi, Zachary Colter, Ehsan Afshari, Ronald G. Dreslinski:
Applications of Artificial Intelligence on the Modeling and Optimization for Analog and Mixed-Signal Circuits: A Review. IEEE Trans. Circuits Syst. I Regul. Pap. 68(6): 2418-2431 (2021)

CoSPARSE: A Software and Hardware Reconfigurable SpMV Framework for Graph Analytics.
Siying Feng, Jiawen Sun, Subhankar Pal, Xin He, Kuba Kaszyk, Dong-Hyeon Park, John Magnus Morton, Trevor N. Mudge, Murray Cole, Michael F. P. O'Boyle, Chaitali Chakrabarti, Ronald G. Dreslinski:

CoSPARSE: A Software and Hardware Reconfigurable SpMV Framework for Graph Analytics. DAC 2021: 949-954

Prodigy: Improving the Memory Latency of Data-Indirect Irregular Workloads Using Hardware-Software Co-Design.
Nishil Talati, Kyle May, Armand Behroozi, Yichen Yang, Kuba Kaszyk, Christos Vasiladiotis, Tarunesh Verma, Lu Li, Brandon Nguyen, Jiawen Sun, John Magnus Morton, Agreen Ahmadi, Todd M. Austin, Michael F. P. O'Boyle, Scott A. Mahlke, Trevor N. Mudge, Ronald G. Dreslinski:

Prodigy: Improving the Memory Latency of Data-Indirect Irregular Workloads Using Hardware-Software Co-Design. HPCA 2021: 654-667

F1: A Fast and Programmable Accelerator for Fully Homomorphic Encryption.
Nikola Samardzic, Axel Feldmann, Aleksandar Krastev, Srinivas Devadas, Ronald G. Dreslinski, Christopher Peikert, Daniel Sánchez:

F1: A Fast and Programmable Accelerator for Fully Homomorphic Encryption. MICRO 2021: 238-252

SparseAdapt: Runtime Control for Sparse Linear Algebra on a Reconfigurable Accelerator.
Subhankar Pal, Aporva Amarnath, Siying Feng, Michael F. P. O'Boyle, Ronald G. Dreslinski, Christophe Dubach:

SparseAdapt: Runtime Control for Sparse Linear Algebra on a Reconfigurable Accelerator. MICRO 2021: 1005-1021

IGOR: Accelerating Byzantine Fault Tolerance for Real-Time Systems with Eager Execution.
Andrew D. Loveless, Ronald G. Dreslinski, Baris Kasikci, Linh Thi Xuan Phan:

IGOR: Accelerating Byzantine Fault Tolerance for Real-Time Systems with Eager Execution. RTAS 2021: 360-373

RISC-V Reward: Building Out-of-Order Processors in a Computer Architecture Design Course with an Open-Source ISA.
Stephen A. Zekany, Jielun Tan, James A. Connelly, Ronald G. Dreslinski:

RISC-V Reward: Building Out-of-Order Processors in a Computer Architecture Design Course with an Open-Source ISA. SIGCSE 2021: 1096-1102

Improving Performance of Flash Based Key-Value Stores Using Storage Class Memory as a Volatile Memory Extension.
Hiwot Tadese Kassa, Jason Akers, Mrinmoy Ghosh, Zhichao Cao, Vaibhav Gogte, Ronald G. Dreslinski:
Improving Performance of Flash Based Key-Value Stores Using Storage Class Memory as a Volatile Memory Extension. USENIX Annual Technical Conference 2021: 821-837

Versa: A Dataflow-Centric Multiprocessor with 36 Systolic ARM Cortex-M4F Cores and a Reconfigurable Crossbar-Memory Hierarchy in 28nm.
Sung Kim, Morteza Fayazi, Alhad Daftardar, Kuan-Yu Chen, Jielun Tan, Subhankar Pal, Tutu Ajayi, Yan Xiong, Trevor N. Mudge, Chaitali Chakrabarti, David T. Blaauw, Ronald G. Dreslinski, Hun-Seok Kim:
Versa: A Dataflow-Centric Multiprocessor with 36 Systolic ARM Cortex-M4F Cores and a Reconfigurable Crossbar-Memory Hierarchy in 28nm. VLSI Circuits 2021: 1-2

Tablext: A Combined Neural Network And Heuristic Based Table Extractor.
Zach Colter, Morteza Fayazi, Zineb Benameur-El, Serafina Kamp, Shuyan Yu, Ronald G. Dreslinski:

Tablext: A Combined Neural Network And Heuristic Based Table Extractor. CoRR abs/2104.11287 (2021)

Versa: A Dataflow-Centric Multiprocessor with 36 Systolic ARM Cortex-M4F Cores and a Reconfigurable Crossbar-Memory Hierarchy in 28nm.
Sung Kim, Morteza Fayazi, Alhad Daftardar, Kuan-Yu Chen, Jielun Tan, Subhankar Pal, Tutu Ajayi, Yan Xiong, Trevor N. Mudge, Chaitali Chakrabarti, David T. Blaauw, Ronald G. Dreslinski, Hun-Seok Kim:
Versa: A Dataflow-Centric Multiprocessor with 36 Systolic ARM Cortex-M4F Cores and a Reconfigurable Crossbar-Memory Hierarchy in 28nm. CoRR abs/2109.03024 (2021)

F1: A Fast and Programmable Accelerator for Fully Homomorphic Encryption (Extended Version).
Axel Feldmann, Nikola Samardzic, Aleksandar Krastev, Srini Devadas, Ronald G. Dreslinski, Karim Eldefrawy, Nicholas Genise, Chris Peikert, Daniel Sánchez:
F1: A Fast and Programmable Accelerator for Fully Homomorphic Encryption (Extended Version). CoRR abs/2109.05371 (2021)

A 7.3 M Output Non-Zeros/J, 11.7 M Output Non-Zeros/GB Reconfigurable Sparse Matrix-Matrix Multiplication Accelerator.
Dong-Hyeon Park, Subhankar Pal, Siying Feng, Paul Gao, Jielun Tan, Austin Rovinski, Shaolin Xie, Chun Zhao, Aporva Amarnath, Timothy Wesley, Jonathan Beaumont, Kuan-Yu Chen, Chaitali Chakrabarti, Michael Bedford Taylor, Trevor N. Mudge, David T. Blaauw, Hun-Seok Kim, Ronald G. Dreslinski:
A 7.3 M Output Non-Zeros/J, 11.7 M Output Non-Zeros/GB Reconfigurable Sparse Matrix-Matrix Multiplication Accelerator. IEEE J. Solid State Circuits 55(4): 933-944 (2020)

Tetris: Using Software/Hardware Co-Design to Enable Handheld, Physics-Limited 3D Plane-Wave Ultrasound Imaging.
Brendan L. West, Jian Zhou, Ronald G. Dreslinski, Oliver D. Kripfgans, J. Brian Fowlkes, Chaitali Chakrabarti, Thomas F. Wenisch:
Tetris: Using Software/Hardware Co-Design to Enable Handheld, Physics-Limited 3D Plane-Wave Ultrasound Imaging. IEEE Trans. Computers 69(8): 1209-1220 (2020)

Transmuter: Bridging the Efficiency Gap using Memory and Dataflow Reconfiguration.
Subhankar Pal, Siying Feng, Dong-Hyeon Park, Sung Kim, Aporva Amarnath, Chi-Sheng Yang, Xin He, Jonathan Beaumont, Kyle May, Yan Xiong, Kuba Kaszyk, John Magnus Morton, Jiawen Sun, Michael F. P. O'Boyle, Murray Cole, Chaitali Chakrabarti, David T. Blaauw, Hun-Seok Kim, Trevor N. Mudge, Ronald G. Dreslinski:
Transmuter: Bridging the Efficiency Gap using Memory and Dataflow Reconfiguration. PACT 2020: 175-190

R2D3: A Reliability Engine for 3D Parallel Systems.
Javad Bagherzadeh, Aporva Amarnath, Jielun Tan, Subhankar Pal, Ronald G. Dreslinski:
R2D3: A Reliability Engine for 3D Parallel Systems. DAC 2020: 1-6

Accelerating Linear Algebra Kernels on a Massively Parallel Reconfigurable Architecture.
A. Soorishetty, Jian Zhou, Subhankar Pal, David T. Blaauw, H. Kim, Trevor N. Mudge, Ronald G. Dreslinski, Chaitali Chakrabarti:
Accelerating Linear Algebra Kernels on a Massively Parallel Reconfigurable Architecture. ICASSP 2020: 1558-1562

Sparse-TPU: adapting systolic arrays for sparse matrices.
Xin He, Subhankar Pal, Aporva Amarnath, Siying Feng, Dong-Hyeon Park, Austin Rovinski, Haojie Ye, Kuan-Yu Chen, Ronald G. Dreslinski, Trevor N. Mudge:
Sparse-TPU: adapting systolic arrays for sparse matrices. ICS 2020: 19:1-19:12

HETSIM: Simulating Large-Scale Heterogeneous Systems using a Trace-driven, Synchronization and Dependency-Aware Framework.
Subhankar Pal, Kuba Kaszyk, Siying Feng, Björn Franke, Murray Cole, Michael F. P. O'Boyle, Trevor N. Mudge, Ronald G. Dreslinski:
HETSIM: Simulating Large-Scale Heterogeneous Systems using a Trace-driven, Synchronization and Dependency-Aware Framework. IISWC 2020: 13-24

Accelerating Deep Neural Network Computation on a Low Power Reconfigurable Architecture.
Yan Xiong, Jian Zhou, Subhankar Pal, David T. Blaauw, H. S. Kim, Trevor N. Mudge, Ronald G. Dreslinski, Chaitali Chakrabarti:
Accelerating Deep Neural Network Computation on a Low Power Reconfigurable Architecture. ISCAS 2020: 1-5

Performance Characterization of Lattice-Based Cryptography Workloads.
Deepika Natarajan, Ronald G. Dreslinski:
Performance Characterization of Lattice-Based Cryptography Workloads. ISPASS 2020: 220-222

CoPTA: Contiguous Pattern Speculating TLB Architecture.
Yichen Yang, Haojie Ye, Yuhan Chen, Xueyang Liu, Nishil Talati, Xin He, Trevor N. Mudge, Ronald G. Dreslinski:
CoPTA: Contiguous Pattern Speculating TLB Architecture. SAMOS 2020: 67-83

Fully-Autonomous SoC Synthesis Using Customizable Cell-Based Analog and Mixed-Signal Circuits Generation.
Tutu Ajayi, Sumanth Kamineni, Morteza Fayazi, Yaswanth K. Cherivirala, Kyumin Kwon, Shourya Gupta, Wenbo Duan, Jeongsup Lee, Chien-Hen Chen, Mehdi Saligane, Dennis Sylvester, David T. Blaauw, Ronald Dreslinski Jr., Benton H. Calhoun, David D. Wentzloff:
Fully-Autonomous SoC Synthesis Using Customizable Cell-Based Analog and Mixed-Signal Circuits Generation. VLSI-SoC (Selected Papers) 2020: 65-85

An Open-source Framework for Autonomous SoC Design with Analog Block Generation.
Tutu Ajayi, Sumanth Kamineni, Yaswanth K. Cherivirala, Morteza Fayazi, Kyumin Kwon, Mehdi Saligane, Shourya Gupta, Chien-Hen Chen, Dennis Sylvester, David T. Blaauw, Ronald G. Dreslinski, Benton H. Calhoun, David D. Wentzloff:
An Open-source Framework for Autonomous SoC Design with Analog Block Generation. VLSI-SOC 2020: 141-146

A 170W Image Signal Processor Enabling Hierarchical Image Recognition for Intelligence at the Edge.
Hyochan An, Siddharth Venkatesan, Sam Schiferl, Tim Wesley, Qirui Zhang, Jingcheng Wang, Kyojin Choo, Shiyu Liu, Bowen Liu, Ziyun Li, Hengfei Zhong, Luyao Gong, David T. Blaauw, Ronald G. Dreslinski, Dennis Sylvester, Hun-Seok Kim:
A 170W Image Signal Processor Enabling Hierarchical Image Recognition for Intelligence at the Edge. VLSI Circuits 2020: 1-2

STOMP: A Tool for Evaluation of Scheduling Policies in Heterogeneous Multi-Processors.
Augusto Vega, Aporva Amarnath, John-David Wellman, Hiwot Kassa, Subhankar Pal, Hubertus Franke, Alper Buyuktosunoglu, Ronald G. Dreslinski, Pradip Bose:
STOMP: A Tool for Evaluation of Scheduling Policies in Heterogeneous Multi-Processors. CoRR abs/2007.14371 (2020)

Optimal and Error-Free Multi-Valued Byzantine Consensus Through Parallel Execution.
Andrew D. Loveless, Ronald G. Dreslinski, Baris Kasikci:

Optimal and Error-Free Multi-Valued Byzantine Consensus Through Parallel Execution. IACR Cryptol. ePrint Arch. 2020: 322 (2020)

Tetris: A Streaming Accelerator for Physics-Limited 3D Plane-Wave Ultrasound Imaging.
Brendan L. West, Jian Zhou, Ronald G. Dreslinski, J. Brian Fowlkes, Oliver Kripfgans, Chaitali Chakrabarti, Thomas F. Wenisch:

Tetris: A Streaming Accelerator for Physics-Limited 3D Plane-Wave Ultrasound Imaging. DAC 2019: 189

3DTUBE: A Design Framework for High-Variation Carbon Nanotube-based Transistor Technology.
Aporva Amarnath, Javad Bagherzadeh, Jielun Tan, Ronald G. Dreslinski:

3DTUBE: A Design Framework for High-Variation Carbon Nanotube-based Transistor Technology. ISLPED 2019: 1-6

Parallelism Analysis of Prominent Desktop Applications: An 18- Year Perspective.
Siying Feng, Subhankar Pal, Yichen Yang, Ronald G. Dreslinski:

Parallelism Analysis of Prominent Desktop Applications: An 18- Year Perspective. ISPASS 2019: 202-211

Classifying Ego-Vehicle Road Maneuvers from Dashcam Video.
Stephen A. Zekany, Ronald G. Dreslinski, Thomas F. Wenisch:

Classifying Ego-Vehicle Road Maneuvers from Dashcam Video. ITSC 2019: 1204-1210

SMART: STT-MRAM architecture for smart activation and sensing.
Byoungchan Oh, Nilmini Abeyratne, Nam Sung Kim, Ronald G. Dreslinski, Trevor N. Mudge:

SMART: STT-MRAM architecture for smart activation and sensing. MEMSYS 2019: 316-330

A 1.4 GHz 695 Giga Risc-V Inst/s 496-Core Manycore Processor With Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS.
Austin Rovinski, Chun Zhao, Khalid Al-Hawaj, Paul Gao, Shaolin Xie, Christopher Torng, Scott Davidson, Aporva Amarnath, Luis Vega, Bandhav Veluri, Anuj Rao, Tutu Ajayi, Julian Puscar, Steve Dai, Ritchie Zhao, Dustin Richmond, Zhiru Zhang, Ian Galton, Christopher Batten, Michael B. Taylor, Ronald G. Dreslinski:
A 1.4 GHz 695 Giga Risc-V Inst/s 496-Core Manycore Processor With Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS. VLSI Circuits 2019: 30-

A 7.3 M Output Non-Zeros/J Sparse Matrix-Matrix Multiplication Accelerator using Memory Reconfiguration in 40 nm.
Subhankar Pal, Dong-Hyeon Park, Siying Feng, Paul Gao, Jielun Tan, Austin Rovinski, Shaolin Xie, Chun Zhao, Aporva Amarnath, Timothy Wesley, Jonathan Beaumont, Kuan-Yu Chen, Chaitali Chakrabarti, Michael B. Taylor, Trevor N. Mudge, David T. Blaauw, Hun-Seok Kim, Ronald G. Dreslinski:

A 7.3 M Output Non-Zeros/J Sparse Matrix-Matrix Multiplication Accelerator using Memory Reconfiguration in 40 nm. VLSI Circuits 2019: 150-

A 1920 × 1080 30-frames/s 2.3 TOPS/W Stereo-Depth Processor for Energy-Efficient Autonomous Navigation of Micro Aerial Vehicles.
Ziyun Li, Qing Dong, Mehdi Saligane, Benjamin P. Kempke, Luyao Gong, Zhengya Zhang, Ronald G. Dreslinski, Dennis Sylvester, David T. Blaauw, Hun-Seok Kim:
A 1920 × 1080 30-frames/s 2.3 TOPS/W Stereo-Depth Processor for Energy-Efficient Autonomous Navigation of Micro Aerial Vehicles. IEEE J. Solid State Circuits 53(1): 76-90 (2018)

The Celerity Open-Source 511-Core RISC-V Tiered Accelerator Fabric: Fast Architectures and Design Methodologies for Fast Chips.
Scott Davidson, Shaolin Xie, Christopher Torng, Khalid Al-Hawaj, Austin Rovinski, Tutu Ajayi, Luis Vega, Chun Zhao, Ritchie Zhao, Steve Dai, Aporva Amarnath, Bandhav Veluri, Paul Gao, Anuj Rao, Gai Liu, Rajesh K. Gupta, Zhiru Zhang, Ronald G. Dreslinski, Christopher Batten, Michael B. Taylor:
The Celerity Open-Source 511-Core RISC-V Tiered Accelerator Fabric: Fast Architectures and Design Methodologies for Fast Chips. IEEE Micro 38(2): 30-41 (2018)

OuterSPACE: An Outer Product Based Sparse Matrix Multiplication Accelerator.
Subhankar Pal, Jonathan Beaumont, Dong-Hyeon Park, Aporva Amarnath, Siying Feng, Chaitali Chakrabarti, Hun-Seok Kim, David T. Blaauw, Trevor N. Mudge, Ronald G. Dreslinski:

OuterSPACE: An Outer Product Based Sparse Matrix Multiplication Accelerator. HPCA 2018: 724-736

A load balancing technique for memory channels.
Byoungchan Oh, Nam Sung Kim, Jeongseob Ahn, Bingchao Li, Ronald G. Dreslinski, Trevor N. Mudge:

A load balancing technique for memory channels. MEMSYS 2018: 55-66

Impact of FinFET on Near-Threshold Voltage Scalability.
Nathaniel Ross Pinckney, Supreet Jeloka, Ronald G. Dreslinski, Trevor N. Mudge, Dennis Sylvester, David T. Blaauw, Lucian Shifren, Brian Cline, Saurabh Sinha:

Impact of FinFET on Near-Threshold Voltage Scalability. IEEE Des. Test 34(2): 31-38 (2017)

Reining in Long Tails in Warehouse-Scale Computers with Quick Voltage Boosting Using Adrenaline.
Chang-Hong Hsu, Yunqi Zhang, Michael A. Laurenzano, David Meisner, Thomas F. Wenisch, Ronald G. Dreslinski, Jason Mars, Lingjia Tang:

Reining in Long Tails in Warehouse-Scale Computers with Quick Voltage Boosting Using Adrenaline. ACM Trans. Comput. Syst. 35(1): 2:1-2:33 (2017)

A Programmable Galois Field Processor for the Internet of Things.
Yajing Chen, Shengshuo Lu, Cheng Fu, David T. Blaauw, Ronald Dreslinski Jr., Trevor N. Mudge, Hun-Seok Kim:

A Programmable Galois Field Processor for the Internet of Things. ISCA 2017: 55-68

A carbon nanotube transistor based RISC-V processor using pass transistor logic.
Aporva Amarnath, Siying Feng, Subhankar Pal, Tutu Ajayi, Austin Rovinski, Ronald G. Dreslinski:

A carbon nanotube transistor based RISC-V processor using pass transistor logic. ISLPED 2017: 1-6

3.7 A 1920×1080 30fps 2.3TOPS/W stereo-depth processor for robust autonomous navigation.
Ziyun Li, Qing Dong, Mehdi Saligane, Benjamin P. Kempke, Shijia Yang, Zhengya Zhang, Ronald G. Dreslinski, Dennis Sylvester, David T. Blaauw, Hun-Seok Kim:

3.7 A 1920×1080 30fps 2.3TOPS/W stereo-depth processor for robust autonomous navigation. ISSCC 2017: 62-63

14.7 A 288μW programmable deep-learning processor with 270KB on-chip weight storage using non-uniform memory hierarchy for mobile intelligence.
Suyoung Bang, Jingcheng Wang, Ziyun Li, Cao Gao, Yejoong Kim, Qing Dong, Yen-Po Chen, Laura Fick, Xun Sun, Ronald G. Dreslinski, Trevor N. Mudge, Hun-Seok Kim, David T. Blaauw, Dennis Sylvester:
14.7 A 288μW programmable deep-learning processor with 270KB on-chip weight storage using non-uniform memory hierarchy for mobile intelligence. ISSCC 2017: 250-251

Energy-Autonomous Wireless Communication for Millimeter-Scale Internet-of-Things Sensor Nodes.
Yajing Chen, Nikolaos Chiotellis, Li-Xuan Chuo, Carl Pfeiffer, Yao Shi, Ronald G. Dreslinski, Anthony Grbic, Trevor N. Mudge, David D. Wentzloff, David T. Blaauw, Hun-Seok Kim:
Energy-Autonomous Wireless Communication for Millimeter-Scale Internet-of-Things Sensor Nodes. IEEE J. Sel. Areas Commun. 34(12): 3962-3977 (2016)

Sirius Implications for Future Warehouse-Scale Computers.
Johann Hauswald, Michael A. Laurenzano, Yunqi Zhang, Cheng Li, Austin Rovinski, Arjun Khurana, Ronald G. Dreslinski, Trevor N. Mudge, Vinicius Petrucci, Lingjia Tang, Jason Mars:
Sirius Implications for Future Warehouse-Scale Computers. IEEE Micro 36(3): 42-53 (2016)

MBus: A System Integration Bus for the Modular Microscale Computing Class.
Pat Pannuto, Yoonmyung Lee, Ye-Sheng Kuo, Zhiyoong Foo, Benjamin P. Kempke, Gyouho Kim, Ronald G. Dreslinski, David T. Blaauw, Prabal Dutta:
MBus: A System Integration Bus for the Modular Microscale Computing Class. IEEE Micro 36(3): 60-70 (2016)

Exploring Fine-Grained Heterogeneity with Composite Cores.
Andrew Lukefahr, Shruti Padmanabha, Reetuparna Das, Faissal M. Sleiman, Ronald G. Dreslinski, Thomas F. Wenisch, Scott A. Mahlke:
Exploring Fine-Grained Heterogeneity with Composite Cores. IEEE Trans. Computers 65(2): 535-547 (2016)

Designing Future Warehouse-Scale Computers for Sirius, an End-to-End Voice and Vision Personal Assistant.
Johann Hauswald, Michael A. Laurenzano, Yunqi Zhang, Hailong Yang, Yiping Kang, Cheng Li, Austin Rovinski, Arjun Khurana, Ronald G. Dreslinski, Trevor N. Mudge, Vinicius Petrucci, Lingjia Tang, Jason Mars:
Designing Future Warehouse-Scale Computers for Sirius, an End-to-End Voice and Vision Personal Assistant. ACM Trans. Comput. Syst. 34(1): 2:1-2:32 (2016)

Near-threshold computing in FinFET technologies: opportunities for improved voltage scalability.
Nathaniel Ross Pinckney, Lucian Shifren, Brian Cline, Saurabh Sinha, Supreet Jeloka, Ronald G. Dreslinski, Trevor N. Mudge, Dennis Sylvester, David T. Blaauw:
Near-threshold computing in FinFET technologies: opportunities for improved voltage scalability. DAC 2016: 76:1-76:6

A low power software-defined-radio baseband processor for the Internet of Things.
Yajing Chen, Shengshuo Lu, Hun-Seok Kim, David T. Blaauw, Ronald G. Dreslinski, Trevor N. Mudge:
A low power software-defined-radio baseband processor for the Internet of Things. HPCA 2016: 40-51

Enhancing DRAM Self-Refresh for Idle Power Reduction.
Byoungchan Oh, Nilmini Abeyratne, Jeongseob Ahn, Ronald G. Dreslinski, Trevor N. Mudge:
Enhancing DRAM Self-Refresh for Idle Power Reduction. ISLPED 2016: 254-259

Checkpointing Exascale Memory Systems with Existing Memory Technologies.
Nilmini Abeyratne, Hsing Min Chen, Byoungchan Oh, Ronald G. Dreslinski, Chaitali Chakrabarti, Trevor N. Mudge:
Checkpointing Exascale Memory Systems with Existing Memory Technologies. MEMSYS 2016: 18-29

Using Graphics Processing Units in an LTE Base Station.
Qi Zheng, Yajing Chen, Hyunseok Lee, Ronald G. Dreslinski, Chaitali Chakrabarti, Achilleas Anastasopoulos, Scott A. Mahlke, Trevor N. Mudge:
Using Graphics Processing Units in an LTE Base Station. J. Signal Process. Syst. 78(1): 35-47 (2015)

Sirius: An Open End-to-End Voice and Vision Personal Assistant and Its Implications for Future Warehouse Scale Computers.
Johann Hauswald, Michael A. Laurenzano, Yunqi Zhang, Cheng Li, Austin Rovinski, Arjun Khurana, Ronald G. Dreslinski, Trevor N. Mudge, Vinicius Petrucci, Lingjia Tang, Jason Mars:
Sirius: An Open End-to-End Voice and Vision Personal Assistant and Its Implications for Future Warehouse Scale Computers. ASPLOS 2015: 223-238

Adrenaline: Pinpointing and reining in tail queries with quick voltage boosting.
Chang-Hong Hsu, Yunqi Zhang, Michael A. Laurenzano, David Meisner, Thomas F. Wenisch, Jason Mars, Lingjia Tang, Ronald G. Dreslinski:
Adrenaline: Pinpointing and reining in tail queries with quick voltage boosting. HPCA 2015: 271-282

DjiNN and Tonic: DNN as a service and its implications for future warehouse scale computers.
Johann Hauswald, Yiping Kang, Michael A. Laurenzano, Quan Chen, Cheng Li, Trevor N. Mudge, Ronald G. Dreslinski, Jason Mars, Lingjia Tang:
DjiNN and Tonic: DNN as a service and its implications for future warehouse scale computers. ISCA 2015: 27-40

MBus: an ultra-low power interconnect bus for next generation nanopower systems.
Pat Pannuto, Yoonmyung Lee, Ye-Sheng Kuo, Zhiyoong Foo, Benjamin P. Kempke, Gyouho Kim, Ronald G. Dreslinski, David T. Blaauw, Prabal Dutta:
MBus: an ultra-low power interconnect bus for next generation nanopower systems. ISCA 2015: 629-641

A study of mobile device utilization.
Cao Gao, Anthony Gutierrez, Madhav Rajan, Ronald G. Dreslinski, Trevor N. Mudge, Carole-Jean Wu:
A study of mobile device utilization. ISPASS 2015: 225-234

WarpPool: sharing requests with inter-warp coalescing for throughput processors.
John Kloosterman, Jonathan Beaumont, Mick Wollman, Ankit Sethia, Ronald G. Dreslinski, Trevor N. Mudge, Scott A. Mahlke:
WarpPool: sharing requests with inter-warp coalescing for throughput processors. MICRO 2015: 433-444

Heterogeneous microarchitectures trump voltage scaling for low-power cores.
Andrew Lukefahr, Shruti Padmanabha, Reetuparna Das, Ronald G. Dreslinski, Thomas F. Wenisch, Scott A. Mahlke:

Heterogeneous microarchitectures trump voltage scaling for low-power cores. PACT 2014: 237-250

Integrated 3D-stacked server designs for increasing physical density of key-value stores.
Anthony Gutierrez, Michael Cieslak, Bharan Giridhar, Ronald G. Dreslinski, Luis Ceze, Trevor N. Mudge:

Integrated 3D-stacked server designs for increasing physical density of key-value stores. ASPLOS 2014: 485-498

VIX: Virtual Input Crossbar for Efficient Switch Allocation.
Supriya Rao, Supreet Jeloka, Reetuparna Das, David T. Blaauw, Ronald G. Dreslinski, Trevor N. Mudge:

VIX: Virtual Input Crossbar for Efficient Switch Allocation. DAC 2014: 103:1-103:6

Quality-of-Service for a High-Radix Switch.
Nilmini Abeyratne, Supreet Jeloka, Yiping Kang, David T. Blaauw, Ronald G. Dreslinski, Reetuparna Das, Trevor N. Mudge:

Quality-of-Service for a High-Radix Switch. DAC 2014: 163:1-163:6

A hybrid approach to offloading mobile image classification.
Johann Hauswald, Thomas Manville, Q. Zheng, Ronald G. Dreslinski, Chaitali Chakrabarti, Trevor N. Mudge:

A hybrid approach to offloading mobile image classification. ICASSP 2014: 8375-8379

Sources of error in full-system simulation.
Anthony Gutierrez, Joseph Pusdesris, Ronald G. Dreslinski, Trevor N. Mudge, Chander Sudanthi, Christopher D. Emmons, Mitchell Hayenga, Nigel C. Paver:

Sources of error in full-system simulation. ISPASS 2014: 13-22

A study of Thread Level Parallelism on mobile devices.
Cao Gao, Anthony Gutierrez, Ronald G. Dreslinski, Trevor N. Mudge, Krisztián Flautner, Geoffrey Blake:

A study of Thread Level Parallelism on mobile devices. ISPASS 2014: 126-127

Hi-Rise: A High-Radix Switch for 3D Integration with Single-Cycle Arbitration.
Supreet Jeloka, Reetuparna Das, Ronald G. Dreslinski, Trevor N. Mudge, David T. Blaauw:

Hi-Rise: A High-Radix Switch for 3D Integration with Single-Cycle Arbitration. MICRO 2014: 471-483

Evaluating private vs. shared last-level caches for energy efficiency in asymmetric multi-cores.
Anthony Gutierrez, Ronald G. Dreslinski, Trevor N. Mudge:

Evaluating private vs. shared last-level caches for energy efficiency in asymmetric multi-cores. ICSAMOS 2014: 191-198

Centip3De: a many-core prototype exploring 3D integration and near-threshold computing.
Ronald G. Dreslinski, David Fick, Bharan Giridhar, Gyouho Kim, Sangwon Seo, Matthew Fojtik, Sudhir Satpathy, Yoonmyung Lee, Daeyeon Kim, Nurrachman Liu, Michael Wieckowski, Gregory K. Chen, Dennis Sylvester, David T. Blaauw, Trevor N. Mudge:

Centip3De: a many-core prototype exploring 3D integration and near-threshold computing. Commun. ACM 56(11): 97-104 (2013)

Centip3De: A Cluster-Based NTC Architecture With 64 ARM Cortex-M3 Cores in 3D Stacked 130 nm CMOS.
David Fick, Ronald G. Dreslinski, Bharan Giridhar, Gyouho Kim, Sangwon Seo, Matthew Fojtik, Sudhir Satpathy, Yoonmyung Lee, Daeyeon Kim, Nurrachman Liu, Michael Wieckowski, Gregory K. Chen, Trevor N. Mudge, David T. Blaauw, Dennis Sylvester:
Centip3De: A Cluster-Based NTC Architecture With 64 ARM Cortex-M3 Cores in 3D Stacked 130 nm CMOS. IEEE J. Solid State Circuits 48(1): 104-117 (2013)

Centip3De: A 64-Core, 3D Stacked Near-Threshold System.
Ronald G. Dreslinski, David Fick, Bharan Giridhar, Gyouho Kim, Sangwon Seo, Matthew Fojtik, Sudhir Satpathy, Yoonmyung Lee, Daeyeon Kim, Nurrachman Liu, Michael Wieckowski, Gregory K. Chen, Dennis Sylvester, David T. Blaauw, Trevor N. Mudge:

Centip3De: A 64-Core, 3D Stacked Near-Threshold System. IEEE Micro 33(2): 8-16 (2013)

Limits of Parallelism and Boosting in Dim Silicon.
Nathaniel Ross Pinckney, Ronald G. Dreslinski, Korey Sewell, David Fick, Trevor N. Mudge, Dennis Sylvester, David T. Blaauw:

Limits of Parallelism and Boosting in Dim Silicon. IEEE Micro 33(5): 30-37 (2013)

Scaling towards kilo-core processors with asymmetric high-radix topologies.
Nilmini Abeyratne, Reetuparna Das, Qingkun Li, Korey Sewell, Bharan Giridhar, Ronald G. Dreslinski, David T. Blaauw, Trevor N. Mudge:

Scaling towards kilo-core processors with asymmetric high-radix topologies. HPCA 2013: 496-507

WiBench: An open source kernel suite for benchmarking wireless systems.
Qi Zheng, Yajing Chen, Ronald G. Dreslinski, Chaitali Chakrabarti, Achilleas Anastasopoulos, Scott A. Mahlke, Trevor N. Mudge:

WiBench: An open source kernel suite for benchmarking wireless systems. IISWC 2013: 123-132

Catnap: energy proportional multiple network-on-chip.
Reetuparna Das, Satish Narayanasamy, Sudhir Satpathy, Ronald G. Dreslinski:

Catnap: energy proportional multiple network-on-chip. ISCA 2013: 320-331

Parallelization techniques for implementing trellis algorithms on graphics processors.
Qi Zheng, Yen-Po Chen, Ronald G. Dreslinski, Chaitali Chakrabarti, Achilleas Anastasopoulos, Scott A. Mahlke, Trevor N. Mudge:

Parallelization techniques for implementing trellis algorithms on graphics processors. ISCAS 2013: 1220-1223

Hardware acceleration for similarity measurement in natural language processing.
Prateek Tandon, Vahed Qazvinian, Jichuan Chang, Parthasarathy Ranganathan, Ronald G. Dreslinski, Thomas F. Wenisch:

Hardware acceleration for similarity measurement in natural language processing. ISLPED 2013: 409-414

Exploring DRAM organizations for energy-efficient and resilient exascale memories.
Bharan Giridhar, Michael Cieslak, Deepankar Duggal, Ronald G. Dreslinski, Hsing Min Chen, Robert Patti, Betina Hold, Chaitali Chakrabarti, Trevor N. Mudge, David T. Blaauw:

Exploring DRAM organizations for energy-efficient and resilient exascale memories. SC 2013: 23:1-23:12

Architecting an LTE base station with graphics processing units.
Qi Zheng, Yen-Po Chen, Ronald G. Dreslinski, Chaitali Chakrabarti, Achilleas Anastasopoulos, Scott A. Mahlke, Trevor N. Mudge:

Architecting an LTE base station with graphics processing units. SiPS 2013: 219-224

Swizzle-Switch Networks for Many-Core Systems.
Korey Sewell, Ronald G. Dreslinski, Thomas Manville, Sudhir Satpathy, Nathaniel Ross Pinckney, Geoffrey Blake, Michael Cieslak, Reetuparna Das, Thomas F. Wenisch, Dennis Sylvester, David T. Blaauw, Trevor N. Mudge:

Swizzle-Switch Networks for Many-Core Systems. IEEE J. Emerg. Sel. Topics Circuits Syst. 2(2): 278-294 (2012)

XPoint cache: scaling existing bus-based coherence protocols for 2D and 3D many-core systems.
Ronald G. Dreslinski, Thomas Manville, Korey Sewell, Reetuparna Das, Nathaniel Ross Pinckney, Sudhir Satpathy, David T. Blaauw, Dennis Sylvester, Trevor N. Mudge:

XPoint cache: scaling existing bus-based coherence protocols for 2D and 3D many-core systems. PACT 2012: 75-86

Lazy cache invalidation for self-modifying codes.
Anthony Gutierrez, Joseph Pusdesris, Ronald G. Dreslinski, Trevor N. Mudge:

Lazy cache invalidation for self-modifying codes. CASES 2012: 151-160

High radix self-arbitrating switch fabric with multiple arbitration schemes and quality of service.
Sudhir Satpathy, Reetuparna Das, Ronald G. Dreslinski, Trevor N. Mudge, Dennis Sylvester, David T. Blaauw:

High radix self-arbitrating switch fabric with multiple arbitration schemes and quality of service. DAC 2012: 406-411

Process variation in near-threshold wide SIMD architectures.
Sangwon Seo, Ronald G. Dreslinski, Mark Woh, Yongjun Park, Chaitali Chakrabarti, Scott A. Mahlke, David T. Blaauw, Trevor N. Mudge:

Process variation in near-threshold wide SIMD architectures. DAC 2012: 980-987

Assessing the performance limits of parallelized near-threshold computing.
Nathaniel Ross Pinckney, Korey Sewell, Ronald G. Dreslinski, David Fick, Trevor N. Mudge, Dennis Sylvester, David T. Blaauw:

Assessing the performance limits of parallelized near-threshold computing. DAC 2012: 1147-1152

Embedded way prediction for last-level caches.
Faissal M. Sleiman, Ronald G. Dreslinski, Thomas F. Wenisch:

Embedded way prediction for last-level caches. ICCD 2012: 167-174

Centip3De: A 3930DMIPS/W configurable near-threshold 3D stacked system with 64 ARM Cortex-M3 cores.
David Fick, Ronald G. Dreslinski, Bharan Giridhar, Gyouho Kim, Sangwon Seo, Matthew Fojtik, Sudhir Satpathy, Yoonmyung Lee, Daeyeon Kim, Nurrachman Liu, Michael Wieckowski, Gregory K. Chen, Trevor N. Mudge, Dennis Sylvester, David T. Blaauw:

Centip3De: A 3930DMIPS/W configurable near-threshold 3D stacked system with 64 ARM Cortex-M3 cores. ISSCC 2012: 190-192

A 4.5Tb/s 3.4Tb/s/W 64×64 switch fabric with self-updating least-recently-granted priority and quality-of-service arbitration in 45nm CMOS.
Sudhir Satpathy, Korey Sewell, Thomas Manville, Yen-Po Chen, Ronald G. Dreslinski, Dennis Sylvester, Trevor N. Mudge, David T. Blaauw:
A 4.5Tb/s 3.4Tb/s/W 64×64 switch fabric with self-updating least-recently-granted priority and quality-of-service arbitration in 45nm CMOS. ISSCC 2012: 478-480

Composite Cores: Pushing Heterogeneity Into a Core.
Andrew Lukefahr, Shruti Padmanabha, Reetuparna Das, Faissal M. Sleiman, Ronald G. Dreslinski, Thomas F. Wenisch, Scott A. Mahlke:

Composite Cores: Pushing Heterogeneity Into a Core. MICRO 2012: 317-328

Low power interconnects for SIMD computers.
Mark Woh, Sudhir Satpathy, Ronald G. Dreslinski, Danny Kershaw, Dennis Sylvester, David T. Blaauw, Trevor N. Mudge:

Low power interconnects for SIMD computers. DATE 2011: 600-605

Bloom Filter Guided Transaction Scheduling.
Geoffrey Blake, Ronald G. Dreslinski, Trevor N. Mudge:

Bloom Filter Guided Transaction Scheduling. HPCA 2011: 75-86

Full-system analysis and characterization of interactive smartphone applications.
Anthony Gutierrez, Ronald G. Dreslinski, Thomas F. Wenisch, Trevor N. Mudge, Ali G. Saidi, Christopher D. Emmons, Nigel C. Paver:

Full-system analysis and characterization of interactive smartphone applications. IISWC 2011: 81-90

Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits.
Ronald G. Dreslinski, Michael Wieckowski, David T. Blaauw, Dennis Sylvester, Trevor N. Mudge:

Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits. Proc. IEEE 98(2): 253-266 (2010)

Evolution of thread-level parallelism in desktop applications.
Geoffrey Blake, Ronald G. Dreslinski, Trevor N. Mudge, Krisztián Flautner:

Evolution of thread-level parallelism in desktop applications. ISCA 2010: 302-313

Diet SODA: a power-efficient processor for digital cameras.
Sangwon Seo, Ronald G. Dreslinski, Mark Woh, Chaitali Chakrabarti, Scott A. Mahlke, Trevor N. Mudge:

Diet SODA: a power-efficient processor for digital cameras. ISLPED 2010: 79-84

A survey of multicore processors.
Geoffrey Blake, Ronald G. Dreslinski, Trevor N. Mudge:

A survey of multicore processors. IEEE Signal Process. Mag. 26(6): 26-37 (2009)